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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,623	08/31/2001	Rami Rahim	0023-0043	8755

44987 7590 03/21/2005

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EXAMINER	
CHOI, WOO H	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,623	RAHIM ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *34-37* is/are withdrawn from consideration.

5)☒ Claim(s) *29-33* is/are allowed.

6)☒ Claim(s) *1,4-6,9,12-15 and 17-25* is/are rejected.

7)☒ Claim(s) *2,3,7,8,10,11,16 and 26-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 17 – 18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Qureshi *et al.* (US Patent No. 5,974,480, hereinafter "Qureshi").

Quereshi discloses a network device, comprising:

a memory configured to store data units (figure 2, 105);

a plurality of request engines (108, 110) configured to generate write requests, the write requests each including at least one data unit; and

at least one memory controller including an address register (figure 3B, 222, see also abstract), the at least one memory controller configured to:

receive a write request (figure 2),

determine where to store the data unit included in the write request using the address register (col. 4, lines 44 – 53), and

store the data unit at a location identified by the address register.

3. With respect to claim 18, a number of the data units comprise a data packet (abstract, requested transfer block) and the at least one memory controller is further configured to:

increment the address register after storing the data unit (abstract, address register is incremented by the data size after the transfer).

4. With respect to claim 22, the write requests include information identifying an amount by which the at least one memory controller is to increment the address register (abstract).

5. Claims 19 – 21, 23 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Seshan *et al.* (US Patent No. 6,145,027, hereinafter "Seshan").

6. With respect to claims 19, 20 and 23, Seshan discloses a method for writing data in a network device, comprising:

generating write requests, each write request including at least one data unit and a number of the data units comprising a data packet (col. 3, lines 56 – 65);

forwarding the write requests to one of a plurality of memory controllers (figure 1B, 141 and 142), each of the memory controllers including an address register (figure 11);

determining, by a first one of the memory controllers, where to stare the data unit using its address register (figure 11, destination address is the target address for a DMA transfer);

storing the data unit at a location identified by the address register; and

incrementing the address register (col. 14, lines 29 – 38).

Seshan also discloses a plurality of memory banks (figure 1B, 22).

7. With respect to claim 21, the write requests do not include information identifying a particular location in one of the plurality of memory banks (the write requests do not include information identifying a particular location in one of the plurality of memory banks that is not a target of the transfer operation).

8. With respect to claim 24, the write requests include information identifying an amount by which to increment the address register (col. 14, lines 29 – 38, element size of the data being transferred identifies the increment value), and the incrementing the address register includes:

incrementing the address register by a first value (size of the data element) or a second value, based on information included in the write request.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 4 – 6, 9, 12 – 15 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Niida *et al.* (US Patent Application Publication No. 2003/0156093, hereinafter "Niida").

11. With respect to claims 1, and 9, Niida discloses a system for writing data (figure 3), comprising:

a memory configured to store data units (304);

at least one memory controller (memory controller of 304) configured to:

receive a first write request associated with a data unit (figure 12, 404),

store the data unit in the memory, and

transmit a first reply (405) including a first address (figure 13, 507, see also page 13, paragraph 254) where the data unit is stored (page 13, paragraph 254); and

control logic configured to:

receive the first reply (figure 12, 405).

However, Niida does not specifically disclose that a control logic is configured to determine whether the first address differs from an address included in at least one other reply by at least a first value. On the other hand, Niida discloses that the destination_offset, i.e., first address, may be the same for all connections or different for different connections (page 14, paragraph 287) and that if they are different, a plurality of connections can efficiently be processed in parallel.

Therefore, it would have been obvious to one of ordinary skill in the art, having the teachings of Niida at the time the invention was made, to determine whether an offset address of a connection is different from the offset address of an existing connection in order to decide

whether parallel operations can be conducted. Niida discloses that connections processed in parallel are efficient (page14, paragraph 287).

12. With respect to claims 4 and 12, the memory comprises a plurality of memory devices and the at least one memory controller comprises a plurality of memory controllers, the system further comprising:

a request engine (figure 12, 302) configured to:

generate the first write request, and

transmit the first write request to a first one of the memory controllers (404); and wherein the first memory controller is configured to determine where to store the data unit associated with the first write request.

13. With respect to claims 5 and 13, the at least one memory controller is configured to increment its address register (figure 13, 514, the Examiner notes that, as claimed, this is merely a location to hold some unspecified address that is not necessarily related to the claimed first address) by a first predetermined value after a data unit is stored.

14. With respect to claims 6 and 14, the at least one memory controller is configured to:

receive a second write request (figure 12, 407) indicating that a value in its address register is outside a predetermined range (figure 5, 514, the sequence number is outside the range of previously transmitted sequence number)

store a second data unit associated with the second write request (transmitted data packet is stored in 304), and

increment its address register by a second predetermined value after the second data unit is stored (the sequence number in the reply packet is updated, see page 15, paragraph 297).

15. With respect to claim 15, the method further comprises:

transmitting a second reply including a second address where the second data unit is stored (figures 3 and 12, Niida discloses multiple connections, a response 405 for a second connection reads on this limitation); and

determining whether the second address differs from an address included in at least one other reply by less than a second value (see rejection of claim 9 above).

16. With respect to claim 25, the differences between this claim and claim 1 are as follows:

a plurality of memory devices (figure 3 shows multiple destinations) and a data packet (figure 5),

address registers associated with memory controllers that identify the data storage location (figure 13, 507, destination offset is where the received data is to be stored and each destination module knows this offset, therefore, the location where this information is stored in 304 corresponds to an address register).

Kiida discloses all of the limitations of claim 1 plus the differences discussed above.

Allowable Subject Matter

17. Claims 29 – 33 are allowed.

18. Claims 2, 3, 7, 8, 10, 11, 16, 26 – 28 are rejected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

19. Applicant's arguments filed December 23, 2004 regarding the restriction requirement have been fully considered but they are not persuasive. The Examiner agrees with Applicant that some dependent claims in Group I recite features associated with incrementing values in an address register. However, the Examiner does not agree that the scope of features recited in Group I is similar to the claimed feature of Group II. First of all, address registers in Group I are part of memory controllers that perform specific functions that are claimed in Group I. In contrast, address incrementing method of Group II applies to any address, making it much broader. Secondly, Group II claims conditional incrementing of an address by one value or another other depending on a condition, while Group I incrementing features have no condition associated with them. For example, claims 5 and 6 require unconditional incrementing by a give value. Likewise, claim 24 only requires unconditional incrementing by one of the two optional values. It does not require that the value be chosen based on a condition.

Since the dominant features of the two Groups are classified in different subclasses and the features that Applicant alleges to be common and similar in scope are not in fact similar in scope and are different as discussed above, the Examiner maintains that the restriction is proper.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Woo H. Choi
March 21, 2005